

REMARKS

Claims 1-49 were originally filed in the present application. Claims 16, 25-28 and 37 are presently amended. No other claims are presently amended, canceled or added. Thus, claims 1-49 remain pending in the present application. Reconsideration of this application in light of the above amendments and the following remarks is requested.

Rejections under 35 U.S.C. §112

Claims 1-15 and 38-49 were rejected under 35 U.S.C. §112, second paragraph, based on alleged inconsistencies. More specifically, the Examiner commented that the last line of each of claims 1, 44 and 47 “states that the S/D regions are coplanar” and that such a coplanar nature is inconsistent with the Examiner’s notation of possible “recessed/extended” combinations. However, the last line of each of claims 1, 44 and 47 recites “second source/drain regions substantially coplanar with the surface.” The last line of each of claims 1, 44 and 47 does not recite “second source/drain regions *and first source/drain regions* substantially coplanar with the surface,” as would be required to support the Examiner’s finding of inconsistency.

Applicants also respectfully note that the possible “recessed/extended” combinations provided by the Examiner are incorrect. For example, it appears the Examiner’s list of possible combinations inadvertently omits combinations in which the second source/drain regions are coplanar with the substrate surface.

The Examiner has also rejected claim 38 for reasons similar to the rejection of claims 1, 44 and 47. However, the last line of claim 38 does not require that both the first source/drain regions and the second source/drain regions be substantially free of SiC and SiGe, as noted by the Examiner. Specifically, the last line of claim 38 provides that the second source/drain regions may substantially not comprise either of SiC and SiGe, but provides no limitation to the composition of the first source/drain regions.

Amendment to the Drawings:

Due to an inadvertent typographical error, the etch stop layer 185 was incorrectly referenced by the reference numeral 180, in paragraph [0025] of the application and in Fig. 1. Consequently, in addition to the amendment to paragraph [0025] described above, the present submittal includes a replacement sheet showing Fig. 1 after amendment to correct the inadvertent typographical error. The present submittal also includes an annotated sheet showing the changes made to Fig. 1 by the present amendment. Both the replacement drawing sheet and the annotated drawing sheet are attached at the end of this paper.

The Applicants appreciate the Examiner's diligence in calling attention to this inadvertent error.

For these reasons, it is believed that claims 1, 38, 44 and 47, as originally filed, are in complete compliance with 35 U.S.C. §112. Consequently, the rejection of these claims under 35 U.S.C. §112 should be withdrawn.

Rejections under 35 U.S.C. §102(e)

Claims 1, 5-7, 11-14, 38 and 44 were rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent Application Publication No. 20040173815, having Yeo, et al., named as inventor (“Yeo ‘815”). However, rejections based on 35 U.S.C. §102(e) cannot be supported by Yeo ‘815 as applied to claims 1, 5-7, 11, 12-14, 38 and 44, for at least the following reasons.

Claim 1

Claim 1 recites:

1. A semiconductor device, comprising:
an isolation region located in a substrate;
an NMOS device located partially over a surface of the substrate;
and
a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface;
wherein a first one of the NMOS and PMOS devices includes one of:
first source/drain regions recessed within the surface; and
first source/drain regions extending from the surface; and
wherein a second one of the NMOS and PMOS devices includes one of:
second source/drain regions recessed within the surface
wherein the first source/drain regions extend from the surface;
second source/drain regions extending from the surface
wherein the first source/drain regions are recessed within the surface; and
second source/drain regions substantially coplanar with the surface.

The PTO provides in MPEP §2131 that:

“[t]o anticipate a claim, the reference must teach every element of the claim.”

Therefore, to support a rejection with respect to claim 1, Yeo ‘815 must contain all of the above-claimed elements of the claim. However, Yeo ‘815 does not disclose an NMOS device and a PMOS device each located partially over a substrate surface, wherein a first one of the NMOS and PMOS devices includes one of: (1) first source/drain regions recessed within the surface, and (2) first source/drain regions extending from the surface; and wherein a second one of the NMOS and PMOS devices includes one of: (1) second source/drain regions recessed within the surface wherein the first source/drain regions extend from the surface; (2) second source/drain regions extending from the surface wherein the first source/drain regions are recessed within the surface; and (3) second source/drain regions substantially coplanar with the surface.

As a result, rejections based on 35 U.S.C. §102(e) cannot be supported by Yeo ‘815 as applied to claim 1.

Claim 38

Claim 38 recites:

38. A semiconductor device, comprising:
an isolation region located in a substrate;
an NMOS device located partially over a surface of the substrate;
and
a PMOS device isolated from the NMOS device by the isolation
region and located partially over the surface;
wherein a first one of the NMOS and PMOS devices includes one
of:
first source/drain regions located at least partially within the
substrate and comprising SiC; and

first source/drain regions located at least partially within the substrate and comprising SiGe; and wherein a second one of the NMOS and PMOS devices includes one of:
second source/drain regions located at least partially within the substrate and comprising SiC wherein the first source/drain regions comprise SiGe;
second source/drain regions located at least partially within the substrate and comprising SiGe wherein the first source/drain regions comprise SiC; and
second source/drain regions located at least partially within the substrate and substantially not comprising either of SiC and SiGe.

Therefore, to support a rejection with respect to claim 38, Yeo '815 must contain all of the above-claimed elements of the claim. However, Yeo '815 does not disclose an NMOS device and a PMOS device each located partially over a substrate surface, wherein a first one of the NMOS and PMOS devices includes one of: (1) first source/drain regions located at least partially within the substrate and comprising SiC; and (2) first source/drain regions located at least partially within the substrate and comprising SiGe; and wherein a second one of the NMOS and PMOS devices includes one of: (1) second source/drain regions located at least partially within the substrate and comprising SiC wherein the first source/drain regions comprise SiGe; (2) second source/drain regions located at least partially within the substrate and comprising SiGe wherein the first source/drain regions comprise SiC; and (3) second source/drain regions located at least partially within the substrate and substantially not comprising either of SiC and SiGe.

As a result, rejections based on 35 U.S.C. §102(e) cannot be supported by Yeo '815 as applied to claim 38.

Claim 44

Claim 44 recites:

44. A method of manufacturing a semiconductor device,
comprising:
forming an isolation region located in a substrate;
forming an NMOS device located partially over a surface of the
substrate; and
forming a PMOS device isolated from the NMOS device by the
isolation region and located partially over the surface;
wherein a first one of the NMOS and PMOS devices includes one
of:
 first source/drain regions recessed within the surface; and
 first source/drain regions extending from the surface; and
wherein a second one of the NMOS and PMOS devices includes
one of:
 second source/drain regions recessed within the surface
 wherein the first source/drain regions extend from the
 surface;
 second source/drain regions extending from the surface
 wherein the first source/drain regions are recessed within
 the surface; and
 second source/drain regions substantially coplanar with the
 surface.

Therefore, to support a rejection with respect to claim 44, Yeo '815 must contain all of the above-claimed elements of the claim. However, Yeo '815 does not disclose forming an NMOS device and a PMOS device each located partially over a substrate surface, wherein a first one of the NMOS and PMOS devices includes one of: (1) first source/drain regions recessed within the surface, and (2) first source/drain regions extending from the surface; and wherein a second one of the NMOS and PMOS devices includes one of: (1) second source/drain regions recessed within the surface wherein the first source/drain regions extend from the surface; (2) second source/drain regions extending from the surface wherein the first source/drain regions are recessed within the surface; and (3) second source/drain regions substantially coplanar with the surface.

As a result, rejections based on 35 U.S.C. §102(e) cannot be supported by Yeo '815 as applied to claim 44.

Rejections under 35 U.S.C. §103(a)

Claims 2-4, 8-10, 15-37, 39-43 and 45-49 were rejected under 35 U.S.C. §103(a) as being unpatentable over one or more of:

- Yeo '815,
- U.S. Patent No. 6,524,938 to Tao, et al. ("Tao"),
- Shimizu, et al., "Local Mechanical Stress Control," IEDM 2001, pp. 433-436 ("Shimizu"),
- U.S. Patent Application Publication No. 20040195646, having Yeo, et al., named as inventor ("Yeo '646"),
- U.S. Patent No. 6,774,409 to Baba, et al. ("Baba"),
- U.S. Patent No. 6,348,390 to Wu ("Wu"), and
- U.S. Patent No. 6,187,641 to Rodder, et al. ("Rodder").

However, rejections based on these references (collectively referred to hereafter as the "References") are not applicable to these claims for the following reasons.

Claim 16

Claim 16 recites:

16. A semiconductor device, comprising:
an isolation region located in a substrate;
an NMOS device located partially over a surface of the substrate;
and
a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface;
wherein a first one of the NMOS and PMOS devices includes:
first source/drain regions located at least partially in the substrate; and

a first gate interposing the first source/drain regions and having a first gate height over the surface; and wherein a second one of the NMOS and PMOS devices includes: second source/drain regions located at least partially in the substrate; and a second gate interposing the second source/drain regions and having a second gate height over the surface, wherein the first and second gate heights are substantially different, where the substantial difference between the first and second gate heights at least indirectly causes a substantial difference in magnitudes of first and second stresses in the first and second source/drain regions, respectively.

As the PTO recognizes in MPEP §2142:

The Examiner bears the initial burden of factually supporting any prima facie conclusion of obviousness. If the examiner does not produce a prima facie case, the applicant is under no obligation to submit evidence of nonobviousness.

The Examiner clearly cannot establish a *prima facie* case of obviousness in connection with claim 16 since 35 U.S.C. §103(a) provides that:

[a] patent may not be obtained ... if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains ... (emphasis added)

Thus, when evaluating a claim for determining obviousness, all limitations of the claim must be evaluated. However, the References, alone or in combination, do not teach an NMOS device and a PMOS device each located partially over a substrate surface, wherein a first one of the NMOS and PMOS devices includes: (1) first source/drain regions located at least partially in the substrate; and (2) a first gate interposing the first source/drain regions and having a first gate height over the surface; and wherein a second one of the NMOS and PMOS devices includes:

(1) second source/drain regions located at least partially in the substrate; and (2) a second gate interposing the second source/drain regions and having a second gate height over the surface, wherein the first and second gate heights are substantially different, where the substantial difference between the first and second gate heights at least indirectly causes a substantial difference in magnitudes of first and second stresses in the first and second source/drain regions, respectively.

Therefore, it is impossible to render obvious the subject matter of claim 16, as a whole, based on any combination of the References, and the above explicit terms of the statute cannot be met. As a result, the Examiner's burden of factually supporting a *prima facie* case of obviousness clearly cannot be met with respect to claim 16, and a rejection under 35 U.S.C. §103(a) is not applicable.

There is still another compelling, and mutually exclusive, reason why the References cannot be combined and applied to reject claim 16 under 35 U.S.C. §103(a).

The PTO also provides in MPEP §2142:

[T]he examiner must step backward in time and into the shoes worn by the hypothetical "person of ordinary skill in the art" when the invention was unknown and just before it was made. In view of all factual information, the examiner must then make a determination whether the claimed invention "as a whole" would have been obvious at that time to that person. ...[I]mpermissible hindsight must be avoided and the legal conclusion must be reached on the basis of the facts gleaned from the prior art.

Here, the References do not teach, or even suggest, the desirability of combination since none teach or suggest providing an NMOS device and a PMOS device each located partially over a substrate surface, wherein a first one of the NMOS and PMOS devices includes: (1) first source/drain regions located at least partially in the substrate; and (2) a first gate interposing the first source/drain regions and having a first gate height over the surface; and wherein a second one of the NMOS and PMOS devices includes: (1) second source/drain regions located at least partially in the substrate; and (2) a second gate interposing the second source/drain regions and

having a second gate height over the surface, wherein the first and second gate heights are substantially different, where the substantial difference between the first and second gate heights at least indirectly causes a substantial difference in magnitudes of first and second stresses in the first and second source/drain regions, respectively.

Thus, none of the References provide any incentive or motivation supporting the desirability of combination. Therefore, there is simply no basis in the art for combining the References to support a 35 U.S.C. §103(a) rejection of claim 16.

Therefore, for this mutually exclusive reason, the Examiner's burden of factually supporting a *prima facie* case of obviousness clearly cannot be met with respect to claim 16, and the rejection under 35 U.S.C. §103(a) is not applicable.

Claim 28

Claim 28 recites:

28. A semiconductor device, comprising:
an isolation region located in a substrate;
an NMOS device located partially over a surface of the substrate;
and
a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface;
wherein a first one of the NMOS and PMOS devices includes:
first source/drain regions located at least partially in the substrate;
a first gate interposing the first source/drain regions; and
first spacers on opposing sides of the first gate and each extending from the first gate to a first width; and
wherein a second one of the NMOS and PMOS devices includes:
second source/drain regions located at least partially in the substrate;
a second gate interposing the second source/drain regions;
and
second spacers on opposing sides of the second gate and each extending from the second gate to a second width,
wherein the first and second widths are substantially

different, where the substantial difference between the first and second widths at least indirectly causes a substantial difference in magnitudes of first and second stresses in the first and second source/drain regions, respectively.

The Examiner clearly cannot establish a *prima facie* case of obviousness in connection with claim 28 since the References, alone or in combination, do not teach an NMOS device and a PMOS device each located partially over a substrate surface, wherein a first one of the NMOS and PMOS devices includes: (1) first source/drain regions located at least partially in the substrate; (2) a first gate interposing the first source/drain regions; and (3) first spacers on opposing sides of the first gate and each extending from the first gate to a first width; and wherein a second one of the NMOS and PMOS devices includes: (1) second source/drain regions located at least partially in the substrate; (2) a second gate interposing the second source/drain regions; and (3) second spacers on opposing sides of the second gate and each extending from the second gate to a second width, wherein the first and second widths are substantially different, where the substantial difference between the first and second widths at least indirectly causes a substantial difference in magnitudes of first and second stresses in the first and second source/drain regions, respectively.

Therefore, it is impossible to render obvious the subject matter of claim 28, as a whole, based on any combination of the References, and the above explicit terms of the statute cannot be met. As a result, the Examiner's burden of factually supporting a *prima facie* case of obviousness clearly cannot be met with respect to claim 28, and a rejection under 35 U.S.C. §103(a) is not applicable.

Another compelling and mutually exclusive reason why the References cannot be combined and applied to reject claim 28 under 35 U.S.C. §103(a) is that the References do not teach, or even suggest, the desirability of combination since none teach or suggest providing an NMOS device and a PMOS device each located partially over a substrate surface, wherein a first one of the NMOS and PMOS devices includes: (1) first source/drain regions located at least

partially in the substrate; (2) a first gate interposing the first source/drain regions; and (3) first spacers on opposing sides of the first gate and each extending from the first gate to a first width; and wherein a second one of the NMOS and PMOS devices includes: (1) second source/drain regions located at least partially in the substrate; (2) a second gate interposing the second source/drain regions; and (3) second spacers on opposing sides of the second gate and each extending from the second gate to a second width, wherein the first and second widths are substantially different, where the substantial difference between the first and second widths at least indirectly causes a substantial difference in magnitudes of first and second stresses in the first and second source/drain regions, respectively.

Thus, none of the References provide any incentive or motivation supporting the desirability of combination. Therefore, there is simply no basis in the art for combining the References to support a 35 U.S.C. §103(a) rejection of claim 28.

Therefore, for each of the above, mutually exclusive reasons, the Examiner's burden of factually supporting a *prima facie* case of obviousness clearly cannot be met with respect to claim 28, and the rejection under 35 U.S.C. §103(a) is not applicable.

Claim 47

Claim 47 recites:

47. (Original) An integrated circuit device, comprising:
a plurality of semiconductor devices each including:
 an isolation region located in a substrate;
 an NMOS device located partially over a surface of the
 substrate; and
 a PMOS device isolated from the NMOS device by the
 isolation region and located partially over the surface;
wherein, in ones of the plurality of semiconductor devices,
 a first one of the NMOS and PMOS devices includes one
 of:
 first source/drain regions recessed within the
 surface; and

first source/drain regions extending from the surface; and
wherein, in ones of the plurality of semiconductor devices, a second one of the NMOS and PMOS devices includes one of:
second source/drain regions recessed within the surface wherein the first source/drain regions extend from the surface;
second source/drain regions extending from the surface wherein the first source/drain regions are recessed within the surface; and
second source/drain regions substantially coplanar with the surface; and
a plurality of interconnects connecting ones of the plurality of semiconductor devices.

The Examiner clearly cannot establish a *prima facie* case of obviousness in connection with claim 47 since the References, alone or in combination, do not teach a plurality of semiconductor devices each including an NMOS device and a PMOS device each located partially over a substrate surface, wherein, in ones of the plurality of semiconductor devices, a first one of the NMOS and PMOS devices includes one of: (1) first source/drain regions recessed within the surface; and (2) first source/drain regions extending from the surface; and wherein, in ones of the plurality of semiconductor devices, a second one of the NMOS and PMOS devices includes one of: (1) second source/drain regions recessed within the surface wherein the first source/drain regions extend from the surface; (2) second source/drain regions extending from the surface wherein the first source/drain regions are recessed within the surface; and (3) second source/drain regions substantially coplanar with the surface.

Therefore, it is impossible to render obvious the subject matter of claim 47, as a whole, based on any combination of the References, and the above explicit terms of the statute cannot be met. As a result, the Examiner's burden of factually supporting a *prima facie* case of obviousness clearly cannot be met with respect to claim 47, and a rejection under 35 U.S.C. §103(a) is not applicable.

Another compelling and mutually exclusive reason why the References cannot be combined and applied to reject claim 47 under 35 U.S.C. §103(a) is that the References do not teach, or even suggest, the desirability of combination since none teach or suggest providing a plurality of semiconductor devices each including an NMOS device and a PMOS device each located partially over a substrate surface, wherein, in ones of the plurality of semiconductor devices, a first one of the NMOS and PMOS devices includes one of: (1) first source/drain regions recessed within the surface; and (2) first source/drain regions extending from the surface; and wherein, in ones of the plurality of semiconductor devices, a second one of the NMOS and PMOS devices includes one of: (1) second source/drain regions recessed within the surface wherein the first source/drain regions extend from the surface; (2) second source/drain regions extending from the surface wherein the first source/drain regions are recessed within the surface; and (3) second source/drain regions substantially coplanar with the surface.

Thus, none of the References provide any incentive or motivation supporting the desirability of combination. Therefore, there is simply no basis in the art for combining the References to support a 35 U.S.C. §103(a) rejection of claim 47.

Therefore, for each of the above, mutually exclusive reasons, the Examiner's burden of factually supporting a *prima facie* case of obviousness clearly cannot be met with respect to claim 47, and the rejection under 35 U.S.C. §103(a) is not applicable.

Conclusion

It is clear from the foregoing that independent claims 1, 16, 28, 38, 44 and 47 are in condition for allowance. Dependent claims 2-15, 17-27, 29-37, 39-43, 45, 46, 48 and 49 depend from and further limit independent claims 1, 16, 28, 38, 44 and 47, in a patentable sense. Therefore, claims 2-15, 17-27, 29-37, 39-43, 45, 46, 48 and 49 are also allowable.

Consequently, an early formal notice of allowance of claims 1-49 is requested.

Respectfully submitted,



Dave R. Hofman
Registration No. 55,272

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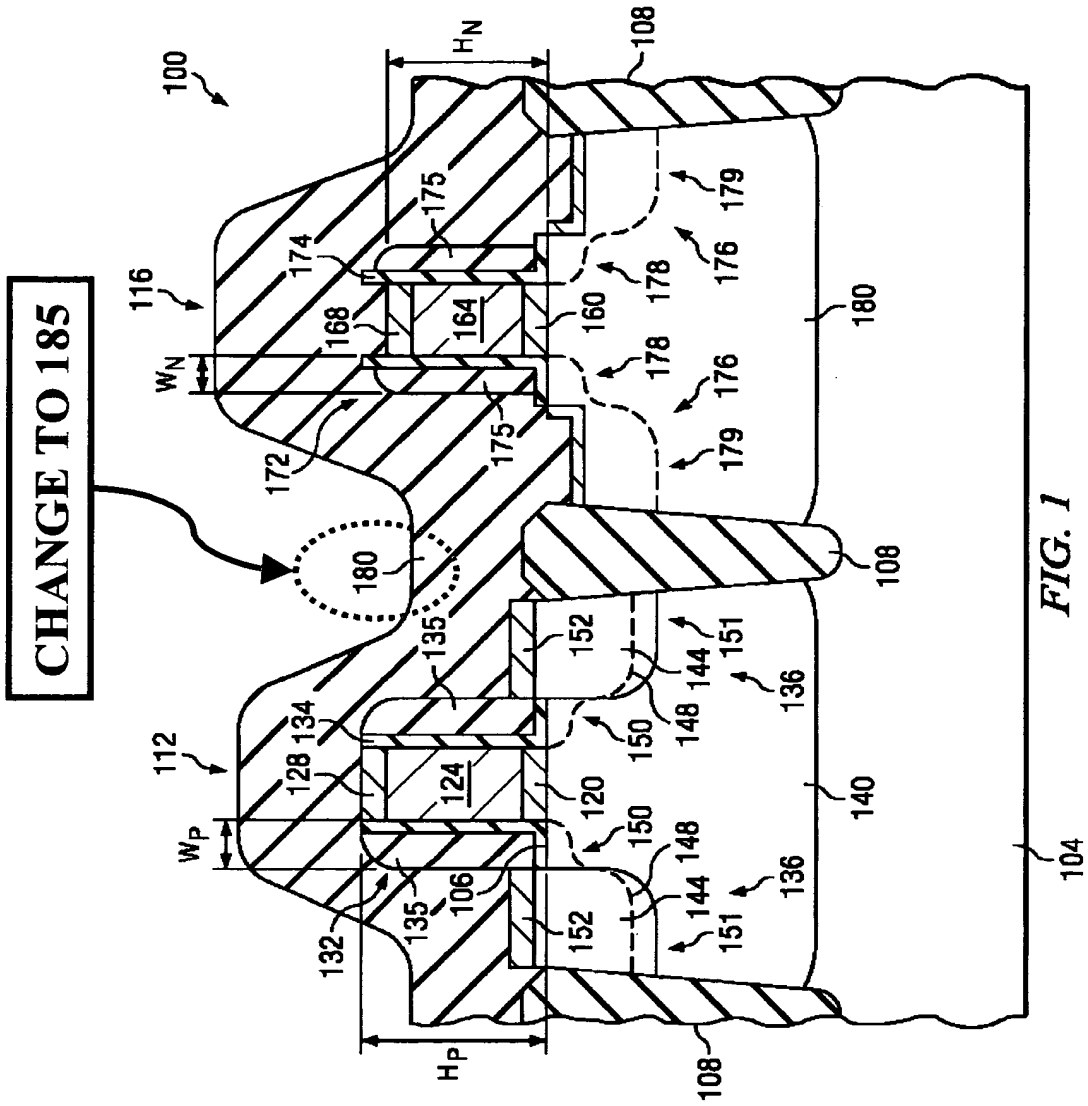
HAYNES AND BOONE, LLP
901 Main Street, Suite 3100
Dallas, Texas 75202-3789
Telephone: 972/739-8630
Facsimile: 214/651-5940
Client Matter No.: 24061.149
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ANNOTATED VERSION WITH MARKINGS SHOWING CHANGES MADE